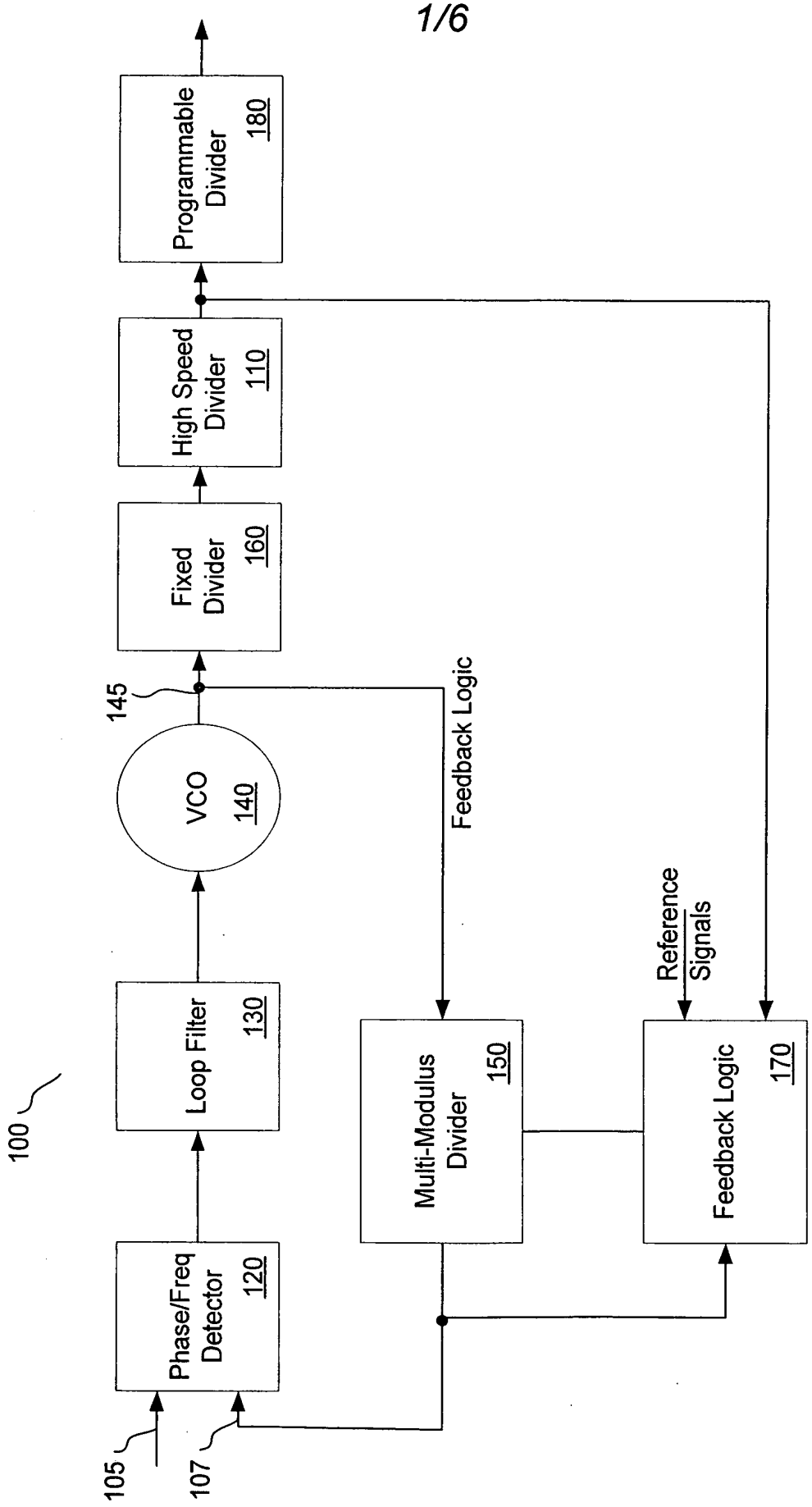
Programmable Divider 180
High Speed Divider 110
Fixed Divider 160
145
VCO 140
Feedback Logic
Loop Filter 130
Reference Signals
Multi-Modulus Divider 150
Feedback Logic 170
100
Phase/Freq Detector 120
105
107

FIG. 1

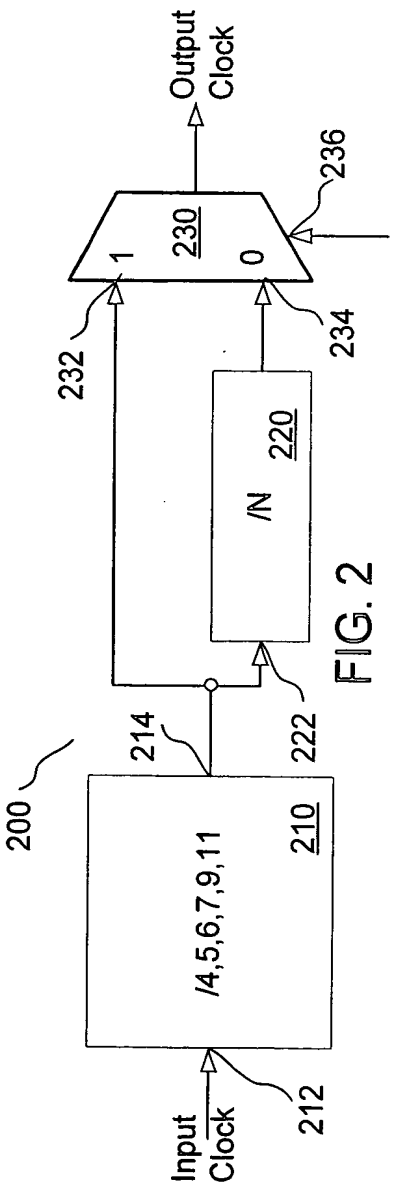
Output Clock
236
230
1
0
232
234
/N 220
214
222
200
/4,5,6,7,9,11 210
Input Clock
212

FIG. 2

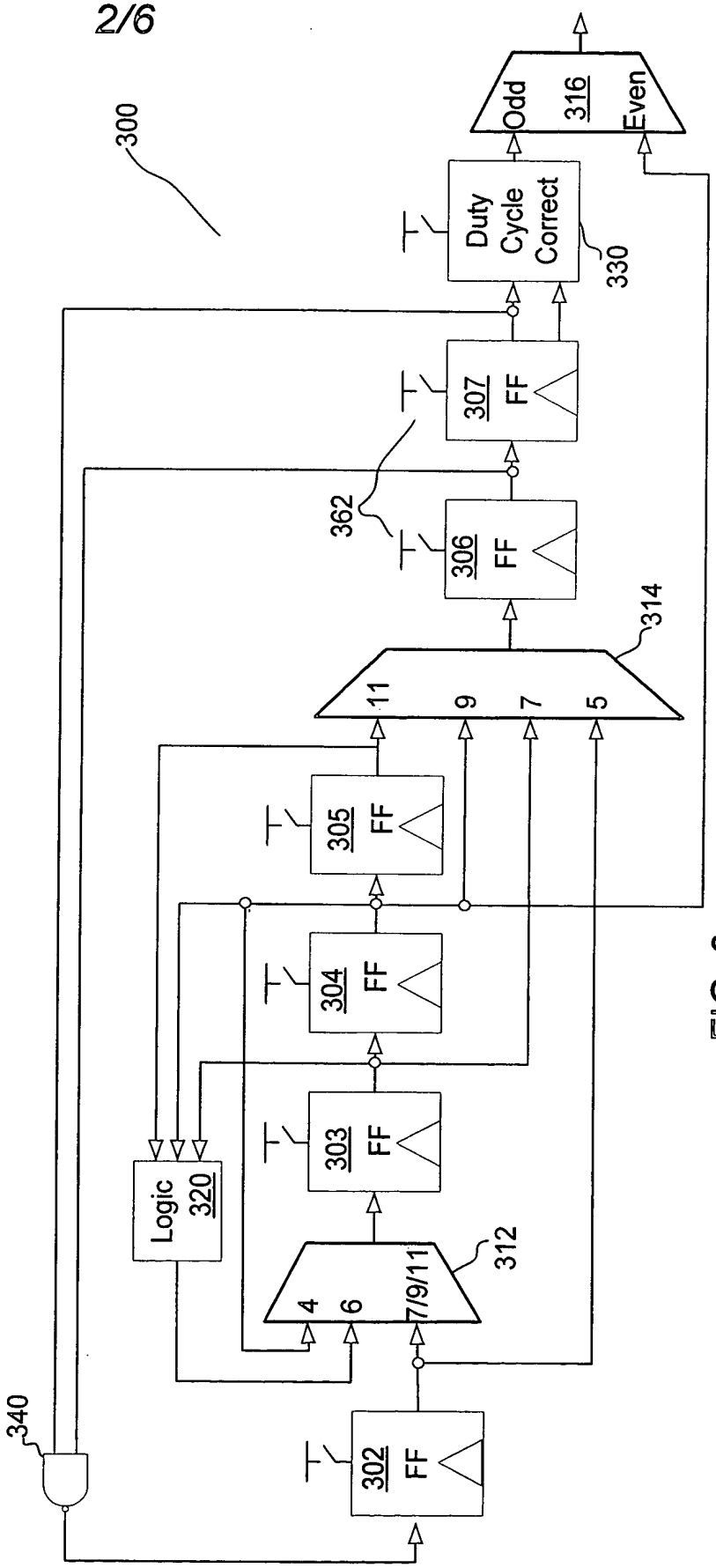
300
Odd 316 Even
Duty Cycle Correct 330
307 FF
362
306 FF
314
11 9 7 5
305 FF
304 FF
303 FF
Logic 320
312
4 6 7/9/11
302 FF
340

FIG. 3

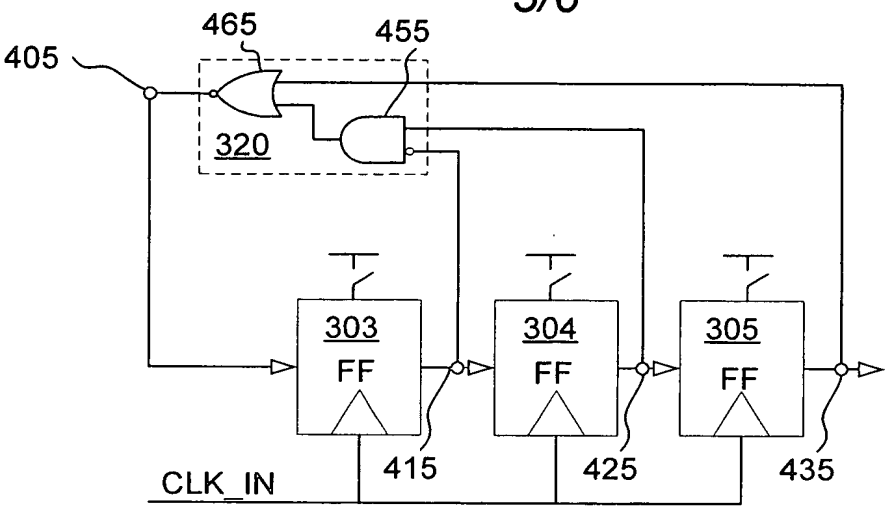

FIG. 4

	415	425	435
Cycle 1	0	0	0
Cycle 2	1	0	0
Cycle 3	1	1	0
Cycle 4	1	1	1
Cycle 5	0	1	1
Cycle 6	0	0	1

FIG. 5

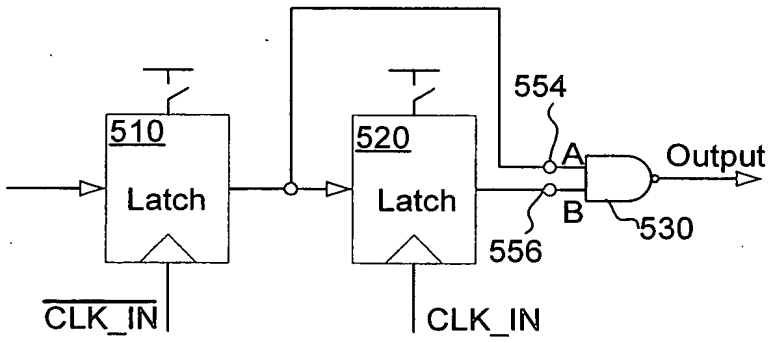

FIG. 6

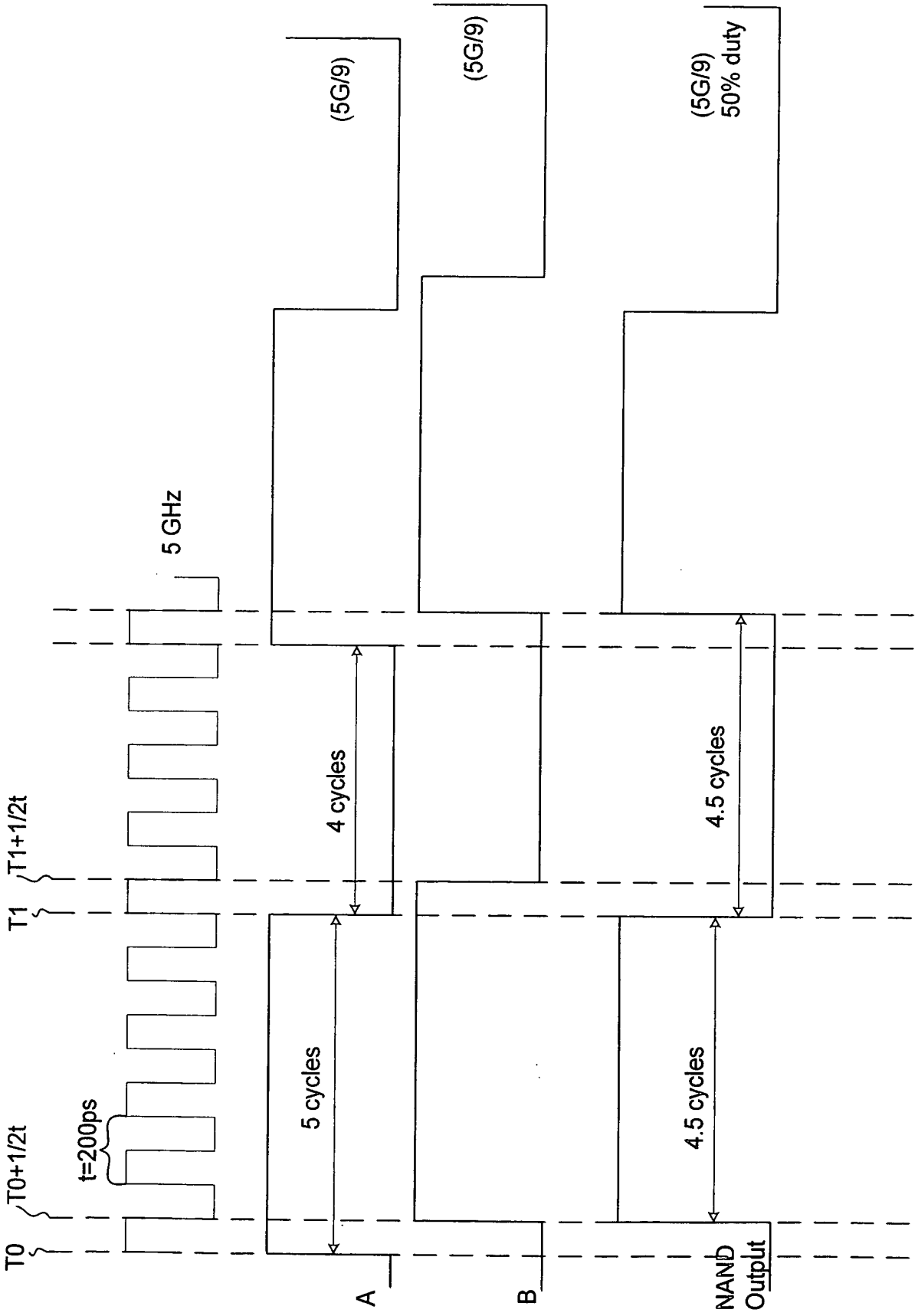
5 GHz
T0
T0+1/2t
t=200ps
T1
T1+1/2t
5 cycles
4 cycles
4.5 cycles
4.5 cycles
A
B
NAND Output
(5G/9)
(5G/9)
(5G/9) 50% duty

FIG. 7

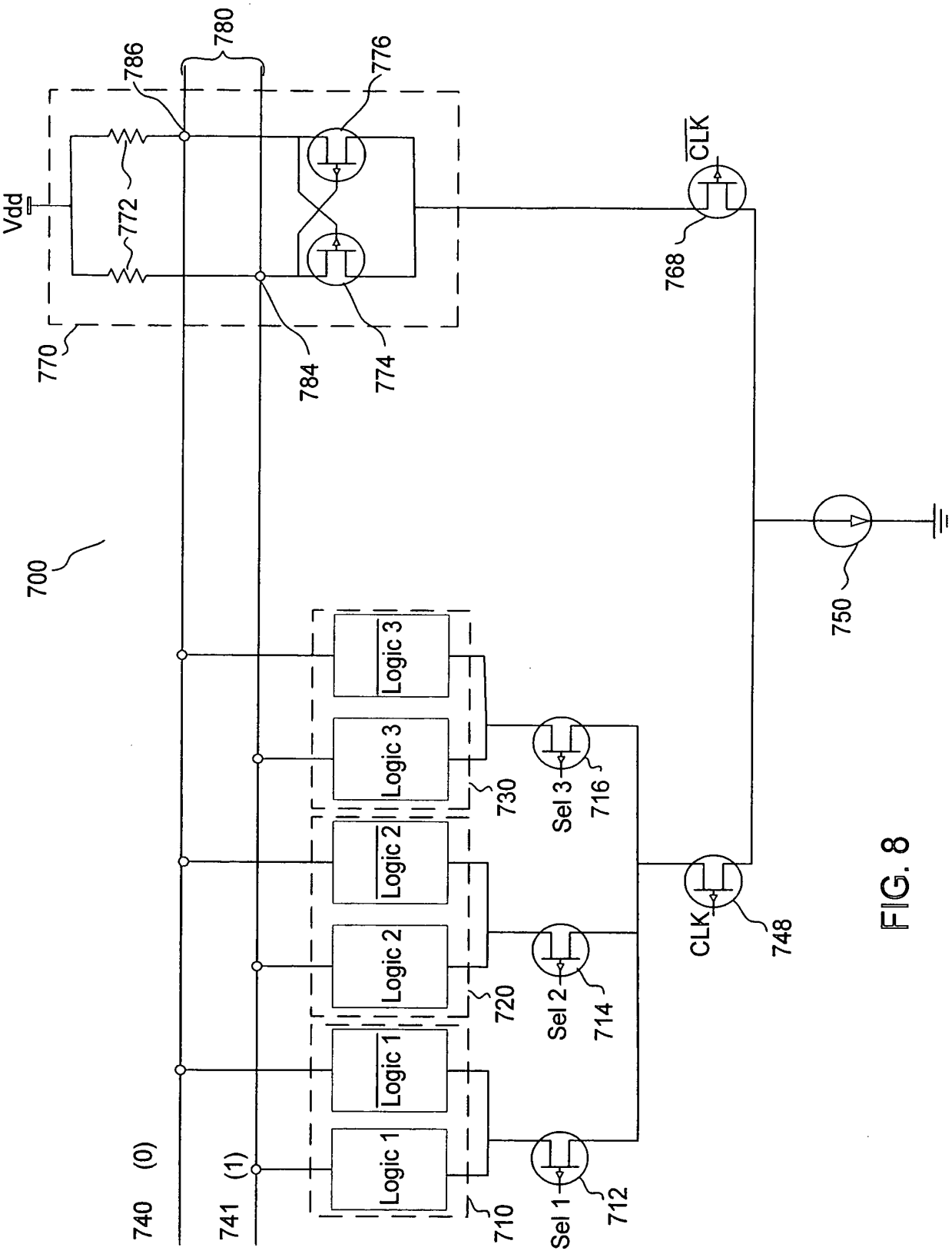
780
786
776
Vdd
772
770
784
774
768
CLK
700
750
Logic 3
Logic 3
730
Sel 3
716
Logic 2
Logic 2
720
Sel 2
714
CLK
748
Logic 1
Logic 1
710
Sel 1
712
740 (0)
741 (1)

FIG. 8

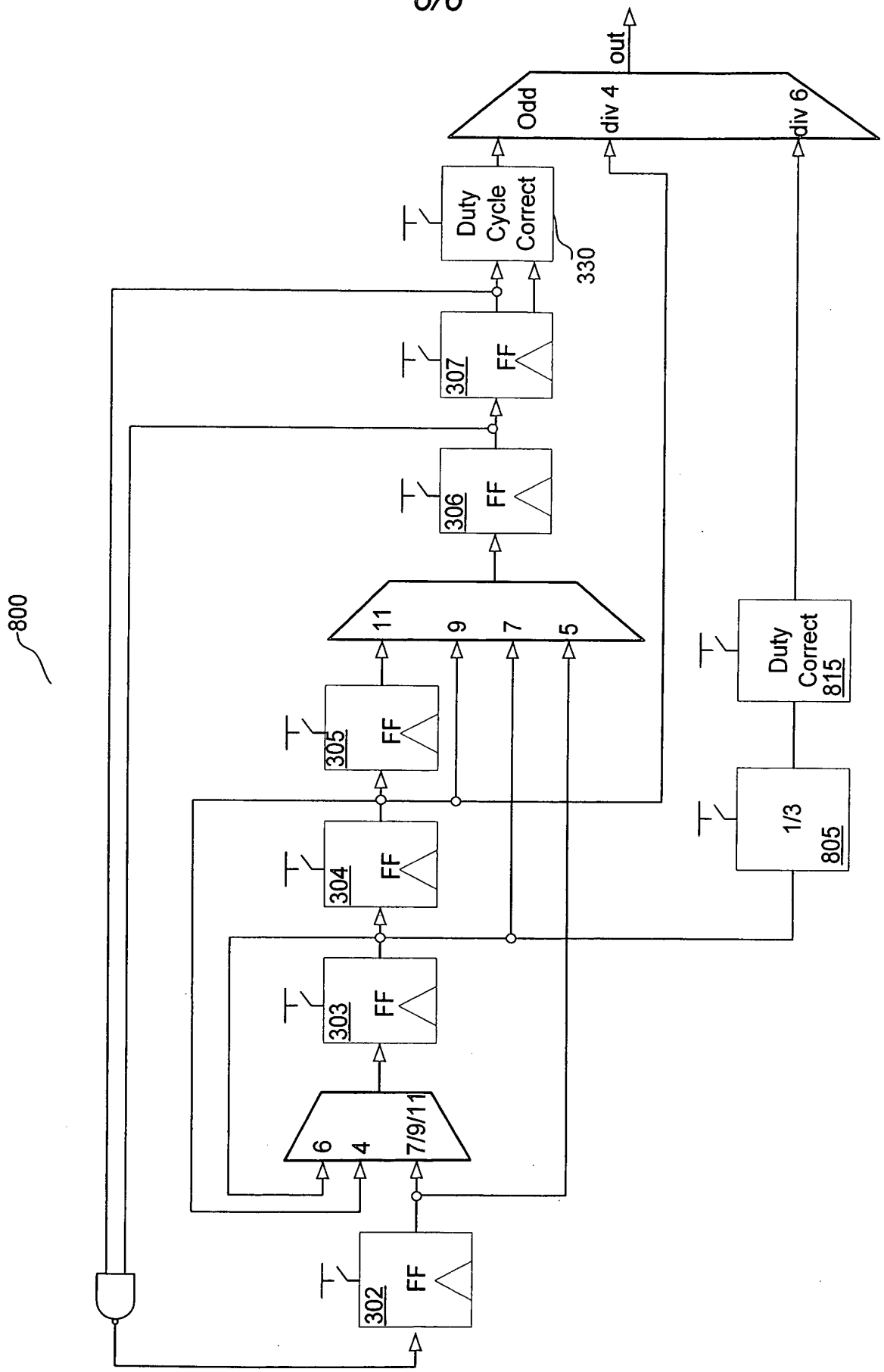
800
out
Odd
div 4
div 6
Duty Cycle Correct
330
307
FF
306
FF
11
9
7
5
305
FF
304
FF
303
FF
6
4
7/9/11
302
FF
Duty Correct
815
1/3
805

FIG. 9